

**Remarks**

Formal acceptance of the above amendments as a submission in connection with USPTO RCE practice is respectfully requested.

In the Substitute Specification, the named paragraphs have been amended to correct minor discovered informalities. Acceptance of these revisions is respectfully requested.

The status of the claims are given hereinabove. Of the currently pending claims, all of the independent claims, i.e., claims 1, 5, 25, 29 and 33, were amended. The currently made amendments to those claims are in consideration of further clarifying that the finally formed gate electrode of a MOS transistor in a semiconductor device according to the present invention is characterized by a stacked structure including four independent layers. In that regard, each of the independent claims, i.e., 1, 5, 25, 29 and 33, was amended to highlight that the claimed metal silicide layer and metal nitride layer are formed as individual layers and that the metal silicide layer of the final stacked structure is provided to function as a contact resistance reducing layer while the metal nitride layer thereof is provided to function as a reaction barrier layer. In connection with further highlighting that these are separate layers on the produced gate structure, the metal silicide layer according to each of the independent claims, as now amended, is defined as having a thickness of 5 to 20 nm. This thickness range was contained in a number of previously pending dependent claims, which are now canceled. It is submitted, the invention as now called for in claims 1+, 5+, 25+, 29+ and 33+, clearly, could not have been anticipated from Weimer et al. It is also submitted, the invention could not have been anticipated " by Applicant Admitted Prior Art (AAPA)." Therefore, insofar as applicable, both of those

rejections are traversed and reconsideration and withdrawal of the same is respectfully requested.

The invention covers a semiconductor device scheme containing one or more MOS transistors and/or including MOS transistors with regard to a CMOS transistor arrangement. With regard to claims 1+ and 25+, the invention calls for a semiconductor device scheme in which the gate electrode of a MOS transistor or of a MOS transistor in connection with a CMOS transistor arrangement is featured as a stacked structure including a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer. The semiconductor device scheme according to claims 5+ and 29+ similarly call for at least such a stacked four-layered gate electrode construction, examples of which are given by the various disclosed embodiments, although not limited thereto. Claims 33+ call for a semiconductor device comprising, on a substrate, one or more MOS transistors, each of which has a gate electrode defined by a stacked structure similarly comprising a silicon layer, a metal silicide layer, a metal nitride layer and a metallic layer, formed in that order beginning with the silicon layer.

In order to highlight that the stacked structure of the formed gate electrode contains four individual layers, each of the above-named independent claimed groups, including claims 1+, 5+, 25+, 29+ and 33+, calls for the metal silicide layer and the metal nitride layer to be formed as individual layers to function as a contact resistance reducing layer and as a reaction barrier layer, respectively, and, in that regard, the metal silicide layer is now specifically defined with a thickness of 5 to 20 nm. The dependent claims further characterize the construction of the gate electrode associated with a MOS transistor or that

pertaining to gate electrodes of complementary MOS transistors.

With regard to the first three disclosed examples in the present application, namely, Figs. 1E, 2D and 3D, the stacked arrangement includes polysilicon layer 103, metal silicide layer 108, metal nitride (reaction barrier) layer 105 and metallic layer 106, in that order, and with regard to the disclosed example fourth and fifth embodiments such as that shown in Figs. 5C and 7B (7C), respectively, the gate electrode stacked layers 311 (312), 320, 308 and 307, in that order, are related thereto (although not limited thereto).

Regarding that featured aspect calling for the metal silicide layer and the metal nitride layer to be formed as individual layers, support directed thereto can be found in the earlier submitted Substitute Specification such as on page 11, lines 12-24, as it relates to disclosed Example 1 embodiment (e.g., Fig. 1E); page 12, lines 11-22 regarding disclosed Example 2 embodiment (e.g., Fig. 2C-2D); page 13, line 19, to page 14, line 2, as it relates to disclosed Example 3 embodiment (e.g., Fig. 3B-3D); page 16, lines 11-15, and page 17, lines 5-10, as it relates to disclosed Example 4 embodiment (e.g., Fig. 5C); and page 18, lines 2-4, and page 19, lines 19-24, as it relates to the disclosed Example 5 embodiment (e.g., Fig. 7B-7C), etc. of the present Specification, although not limited thereto. As can be seen from the above related discussion, the metal silicide layer as well as the metal nitride layer are formed as individual layers of the produced stacked gate structure of a MOS transistor. With the formation of the metal silicide layer, the contact resistance is reduced significantly. It is submitted, such a scheme as that now called for in claims 1+, 5+, 25+, 29+ and 33+ not only was not disclosed by Weimer et al but, moreover, could not have been suggested therefrom. Such is also the case with regard to the presently cited "Applicant Admitted Prior Art

(AAPA)."

Claims 1-8 and 17-40 were finally rejected "for the same reason as set forth in the previous Office Action ...," namely, in which the claims were rejected under 35 USC §102(e) over Weimer et al. In that regard, it is argued on page 3 of the standing Final Office Action that Weimer et al did, in fact, disclose a four-layered structure as that claimed "since Weimer discloses a metal silicide layer (column 4, lines 25-29) and the anneal step forms a barrier layer that contains clearly two layers Wsix (silicide) and SiN (column 4, lines 39-40)." However, as will be shown hereinbelow, Weimer et al's gate construction does not feature a four-layered structure as that presently called for in each of the independent claims 1, 5, 25, 29 and 33.

According to Weimer et al's disclosure, the multi-layered structure is effective for reducing oxidation, agglomeration and silicidation of layers in the conductive structure (see column 1, lines 54-57). Weimer et al's conductive structure, fundamentally, is a vertically stacked gate electrode structure (e.g., 112, in Fig. 1) composed of only three (3) layers, namely, metallic layer 100, as a top conductive layer, an intermediate diffusion barrier layer 102 and a bottom conductive layer 104. (Column 2, line 65, to column 3, line 5, etc., in Weimer et al.) The barrier layer 102 acts to prevent agglomeration of silicon from the bottom layer 104 into the top conductive layer 100. (Column 3, line 6 - 13, in Weimer et al.) When a layer of TiSi or WSi is formed, the resistance is increased. However, the final gate construction only includes a barrier layer inbetween that of the top conductive layer 100 and the bottom layer 104. As explained in Weimer et al, the formation of metal silicide barrier layer relates only to the formation of the barrier

layer itself and, it is submitted, does not involve an additional layer to that of the barrier layer 102.

According to the present invention as now called for in each of the independent claims 1, 5, 25, 29 and 33, the stacked gate structure of a MOS transistor features four independent layers, namely, a metal layer/a reaction barrier layer (for preventing reaction of the metal and silicon)/a metal silicide layer (for reducing the contact resistance)/a silicon layer. Such, it is submitted, was clearly neither taught nor suggested by Weimer et al.

For purposes of this discussion, let us assume that a vertically stacked gate electrode construction for a MOS transistor contains only a reaction barrier layer such as the diffusion barrier layer 102 of Weimer et al between the lower silicon (polysilicon) layer and the top metal conductive layer, which is also the case in connection with the discussed conventional technology in the background discussion of the present application. When only a reaction barrier layer is formed between the silicon and the metal so as to prevent a reaction between the metal and the silicon during the heat treatment, a problem arises of an increased contact resistance between the reaction barrier layer and the silicon. This problem is referred-to in connection with a conventional scheme such as the admitted prior art discussed in the background portion of the present Specification. (Page 2, line 13, to page 3, line 6, of the Substitute Specification.) In order to solve such a problem, the present inventors have schemed a four-layer structure by forming a reaction barrier layer between the top metal layer and the lowermost silicon layer and further forming a metal silicide layer independently thereof between the reaction barrier layer and the silicon. (Page 3, lines 9-19, etc., of the Substitute Specification.)

As to support for the set forth thickness range of the metal silicide layer of the stacked gate electrode structure as that now called for in each of independent claims 1, 5, 25, 29 and 33, example discussion thereof is found on page 6, lines 13-15, on page 7, lines 5-7, etc., of the Substitute Specification. The metal nitride layer and the metal silicide layer are included, as was shown hereinabove, in the various disclosed example embodiments as independent layers in stacked gate structures in the finally constructed device. Such, it is submitted, was neither disclosed nor suggested by either Weimer et al or, for that matter, by the known conventional approach discussed in the background portion of the present application.

Weimer et al, it is submitted, neither disclosed nor was concerned with the idea of forming a metal silicide layer in addition to and independently of forming the reaction barrier layer. As mentioned earlier, Weimer et al forms a conductive diffusion barrier layer 102 (which can be said to be similar to the metal diffusion barrier layer of the present invention) that is resistant to oxidation, agglomeration and silicidation. (Column 3, lines 2-5, in Weimer et al.) It is alleged, in the Final Office Action rejection, that the "anneal step forms a barrier layer that contains clearly two layers Wsix (silicide) and SiN (column 4, lines 39-40)." From a careful study of Weimer et al's disclosure and including from a reading of the description in column 4, lines 39-40 thereof, the barrier layer in Weimer et al's stacked structure is actually one layer that contains Wsix and SiN and is not two layers. This is evident from the use of "a" in the expression the anneal step forms "a" barrier layer that contains Wsix and SiN. Even if two layers may exist during an intermediate step in the manufacture of the stacked structure, the finally

formed stacked gate construction is a WsixNy barrier layer 102 such as noted in column 4, lines 55-58, in Weimer et al, which reads as follows:

*"After anneal in the NH<sub>3</sub>, the layers formed include a tungsten layer 100 at the top and a Wsixny barrier layer 102 between the top tungsten layer and the bottom conductive layer 104."*

As can be seen from this (see also column 4, lines 30-31), Weimer et al's disclosure is strictly directed to the formation of a three-layer construction such as that mentioned in column 2, lines 58-60 thereof.

Practically, it is technically difficult to make one layer such as Weimer et al's diffusion barrier layer 102 to have a multi-functional role, that is, to have Weimer et al's barrier layer function as a reaction barrier layer and, at the same time, function as a contact resistance reducing layer. It is submitted, the three-layer structure according to Weimer et al leads to an increase in the contact resistance thereby lowering its effectiveness such as in connection with LSI application. At least for the above reasons, the invention according to claims 1, 2, 4-6, 8, 17, 18, 20-23, 25, 26, 28-31, 33, 34, 36-38 and 40 could not have been anticipated by Weimer et al or, for that matter, by prior conventional schemes referred to in the background portion of the present application. Moreover, for at least the above reasons, the invention also could not have been rendered obvious therefrom.

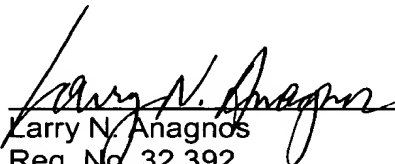
Therefore, in view of the amendments presented hereinabove, together with these accompanying remarks, reconsideration as well as favorable action on all of the presently pending claims and an early formal Notification of Allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under

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37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.40010X00), and please credit any excess fees to such deposit account.

Respectfully submitted,  
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